REMARKS

Claims 1 and 5 are rejected as obvious over USP 6,587,454 ("Lamb") in view of USP 7,023,868 ("Rabenko"). Claims 4, 6 and 10 are rejected as obvious over Lamb and Rabenko in view of US Publication 2006/0072552 ("Shnitzer"). Claims 8-9 and 12-16 are rejected as obvious over Lamb in view of Shnitzer and Rabenko in view of USP 6,574,213 ("Anandakumar"). Claim 17 is rejected as obvious over Lamb in view of Shnitzer, Rabenko and Anandakumar in view of USP 6,449,269 ("Edholm").

The claims have been significantly amended, without prejudice to filing broader claims or continuation applications.

The Examiner's characterization of Lamb and interpretation of the claim limitations is contrary to the understanding of a person of ordinary skill. Although an Examiner is entitled to give the claims the broadest reasonable interpretation, that interpretation must correspond to the understanding of a person of ordinary skill. The Examiner is not free to arbitrarily assign new definitions for well understood terms.

Claim 1 calls for a processing core to control the processor, the processor core including one or more pipelines to execute instructions. The Examiner characterized the MAC/DSP circuit 73 as a processing core. This clearly incorrect, given that Lamb identifies element 75 as the core logic. The Examiner characterized the core node logic 75 as a bus. This is clearly incorrect. The differences between a bus and core logic are so well understood by those of ordinary skill of computing that the Examiner's characterization is bizarre. The Examiner characterizes the connection between the MAC/DSP 73 and the node core logic 75 as a pipeline. This is clearly incorrect. A pipeline is well understood term in the field of computing. A mere electrical connection is not a pipeline.

The Examiner argued that the node core logic 75 provided a repeater that was connected through the node core logic, i.e., connected through itself. This is contradictory and inexplicable.

Claim 1 now recites that the instructions are configured such that when executed by the processing core, PCM coded speech data received by the PCM interface is transported to the external memory, read from the external memory by the processing core and compressed by the

processing core and written back to the external memory, and voice data packets with such speech data are read from the external memory and forwarded to the 802.3 MAC and fed into the external network by the repeater, and voice data packets received by the Ethernet interface are transported to the external memory, read from the external memory by the processing core and decompressed by the processing core and written back to the external memory, and PCM coded speech data from the received voice data packets is transported by the PCM interface to the external voice codec.

This is not shown by Lamb, Shnitzer, Rabenko, Anandakumar or Edholm.

Conclusion

For the foregoing reasons, the applicant submits that all the claims are in condition for allowance.

By responding in the foregoing remarks only to particular positions taken by the examiner, the applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, the applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

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Respectfully submitted,

Date: 10/31/07

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